(FILE 'USPAT' ENTERED AT 11:01:50 ON 11 JUN 1999)

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L1          924 S SUPERSCALAR
                SET HIGH OFF
L2          924 S L1
                SET HIGH ON
L3          247 S (REGISTER "FILE" (4A) (STORE OR WRITE OR READ)) AND L1
L4           93 S (FLOATING POINT (4A) INTEGER) (5A) (REGISTER "FILE")
L5           34 S L4 AND L3
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1. 5,903,772, May 11, 1999, Plural operand buses of intermediate widths coupling to narrower width integer and wider width floating point **superscalar** processing core; Scott A. White, et al., 712/33 [IMAGE AVAILABLE]

2. 5,884,061, Mar. 16, 1999, Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle; James Henry Hesson, et al., 712/217 [IMAGE AVAILABLE]

3. 5,875,315, Feb. 23, 1999, Parallel and scalable instruction scanning unit; Rammohan Narayan, 712/204 [IMAGE AVAILABLE]

4. 5,867,683, Feb. 2, 1999, Method of operating a high performance **superscalar** microprocessor including a common reorder buffer and common **register** **file** for both **integer** and **floating** **point** operations; David B. Witt, et al., 712/218; 395/391, 393, 800.23; 711/147; 712/23, 215, 217 [IMAGE AVAILABLE]

5. 5,867,682, Feb. 2, 1999, High performance **superscalar** microprocessor including a circuit for converting CISC instructions to RISC operations; David B. Witt, et al., 712/210; 395/376, 586; 711/147; 712/200, 239 [IMAGE AVAILABLE]

6. 5,857,096, Jan. 5, 1999, Microarchitecture for implementing an instruction to clear the tags of a stack reference register file; David Bistry, et al., 712/229; 395/378, 569, 678, 800.23; 712/23, 202, 228 [IMAGE AVAILABLE]

7. 5,857,089, Jan. 5, 1999, Floating point stack and exchange instruction; Michael D. Goddard, et al., 712/222; 395/566; 712/225 [IMAGE AVAILABLE]

8. 5,835,748, Nov. 10, 1998, Method for executing different sets of instructions that cause a processor to perform different data type operations on different physical registers files that logically appear to software as a single aliased register file; Doron Orenstein, et al., 712/217, 23, 229, 244 [IMAGE AVAILABLE]

9. 5,832,292, Nov. 3, 1998, High-performance **superscalar**-based computer system with out-of-order instruction execution and concurrent results distribution; Le Trong Nguyen, et al., 712/23, 218 [IMAGE AVAILABLE]

10. 5,826,055, Oct. 20, 1998, System and method for retiring

11. 5,809,276, Sep. 15, 1998, System and method for register renaming; Trevor A. Deosaran, et al., 712/217, 207, 208, 209, 210, 211, 212 [IMAGE AVAILABLE]

12. 5,805,853, Sep. 8, 1998, **Superscalar** microprocessor including flag operand renaming and forwarding apparatus; Scott A. White, et al., 712/218, 23, 215 [IMAGE AVAILABLE]

13. 5,764,938, Jun. 9, 1998, Resynchronization of a **superscalar** processor; Scott A. White, et al., 712/200 [IMAGE AVAILABLE]

14. 5,758,112, May 26, 1998, Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction; Kenneth C. Yeager, et al., 712/217 [IMAGE AVAILABLE]

15. 5,751,981, May 12, 1998, High performance **superscalar** microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format; David B. Witt, et al., 712/204; 711/201; 712/200, 210, 211, 215, 218 [IMAGE AVAILABLE]

16. 5,737,629, Apr. 7, 1998, Dependency checking and forwarding of variable width operands; Gerald D. Zuraski, Jr., et al., 712/23, 216 [IMAGE AVAILABLE]

17. 5,696,955, Dec. 9, 1997, Floating point stack and exchange instruction; Michael D. Goddard, et al., 712/222, 225 [IMAGE AVAILABLE]

18. 5,689,720, Nov. 18, 1997, High-performance **superscalar**-based computer system with out-of-order instruction execution; Le Trong Nguyen, et al., 712/23, 200, 206, 207, 215, 228, 230, 235 [IMAGE AVAILABLE]

19. 5,689,693, Nov. 18, 1997, Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead; Scott A. White, 712/224, 218 [IMAGE AVAILABLE]

20. 5,664,136, Sep. 2, 1997, High performance **superscalar** microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations; David B. Witt, et al., 712/208, 200, 212, 215 [IMAGE AVAILABLE]

21. 5,659,782, Aug. 19, 1997, System and method for handling load and/or store operations in a **superscalar** microprocessor; Cheryl D. Senter, et al., 712/23; 364/DIG.1, DIG.2; 712/41, 200 [IMAGE AVAILABLE]

22. 5,655,098, Aug. 5, 1997, High performance **superscalar** microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format; David B. Witt, et al., 712/210; 711/201; 712/200, 204, 213, 239 [IMAGE AVAILABLE]

23. 5,655,097, Aug. 5, 1997, High performance **superscalar** microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format; David B. Witt, et al., 712/204; 711/147; 712/200, 206, 210 [IMAGE AVAILABLE]

24. 5,651,125, Jul. 22, 1997, High performance **superscalar** microprocessor including a common reorder buffer and common **register**

file for both **integer** and **floating** **point** operations; David B. Witt, et al., 712/218; 710/126; 711/146; 712/215, 217 [IMAGE AVAILABLE]

25. 5,649,225, Jul. 15, 1997, Resynchronization of a **superscalar** processor; Scott A. White, et al., 712/23; 364/231.8, 948.34, DIG.1, DIG.2; 712/1 [IMAGE AVAILABLE]

26. 5,634,118, May 27, 1997, Splitting a floating-point stack-exchange instruction for merging into surrounding instructions by operand translation; James S. Blomgren, 712/226, 23, 202, 222 [IMAGE AVAILABLE]

27. 5,632,023, May 20, 1997, **Superscalar** microprocessor including flag operand renaming and forwarding apparatus; Scott A. White, et al., 712/218, 23, 215 [IMAGE AVAILABLE]

28. 5,625,789, Apr. 29, 1997, Apparatus for source operand dependendency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle; James H. Hesson, et al., 712/217, 218 [IMAGE AVAILABLE]

29. 5,590,352, Dec. 31, 1996, Dependency checking and forwarding of variable width operands; Gerald D. Zuraski, Jr., et al., 712/23; 364/259.2, 263, 263.1, DIG.1 [IMAGE AVAILABLE]

30. 5,590,295, Dec. 31, 1996, System and method for register renaming; Trevor A. Deosaran, et al., 712/217 [IMAGE AVAILABLE]

31. 5,574,928, Nov. 12, 1996, Mixed integer/floating point processor core for a **superscalar** microprocessor with a plurality of operand buses for transferring operand segments; Scott A. White, et al., 712/23; 708/495; 710/126; 712/200; 714/50 [IMAGE AVAILABLE]

32. 5,560,032, Sep. 24, 1996, High-performance, **superscalar**-based computer system with out-of-order instruction execution and concurrent results distribution; Le Trong Nguyen, et al., 712/23; 364/931.11, 931.41, 931.55, DIG.2; 712/217, 218 [IMAGE AVAILABLE]

33. 5,557,763, Sep. 17, 1996, System for handling load and/or store operations in a **superscalar** microprocessor; Cheryl D. Senter, et al., 712/23; 364/DIG.1, DIG.2; 711/140, 169; 712/209 [IMAGE AVAILABLE]

34. 5,539,911, Jul. 23, 1996, High-performance, **superscalar**-based computer system with out-of-order instruction execution; Le T. Nguyen, et al., 712/23 [IMAGE AVAILABLE]

=>

	L #	Hits
1	L2	232
2	L3	128
3	L5	66
4	L1	1323

12-14

	Search Text
1	(register adj file) adj4 (store or write or read) and 1
2	(register adj file) near4 ((floating adj point) or floatingpoint) near5 integer
3	2 and 3
4	superscal$2